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# App Note 366: DS3134 CHATEAU Test Registers

*Application note 366 provides a list of DS3134 CHATEAU internal test registers. The user is recommended to check these registers after a soft system reset. The user should avoid using these registers.*

CHATEAU design follows the main stream Verilog Synopsis flow, and there is a lot of built in test function within the design.

Following is a list of registers users need to avoid. These registers will be reset to "0"s upon power on (hardware) reset or soft system reset. It is recommended to check these registers after soft system reset. All of these registers are 16 bits registers.

**Table 1. CHATEAU Internal Test Register**

| Address (h) | Value (h) |
|---|---|
| 0050 | 0000 |
| 04F0 - 04FF | 0000 |
| 07FD - 07FF | 0000 |
| 08FD - 08FF | 0000 |
| 09F8 - 09FF | 0000 |

Register address 0050h bit 0 is the FT (factory test mode). All the other registers shown in the above table are for CHATEAU internal (Dallas Semiconductor) tests only, not user test mode controls. Values of these bits should always be "0". If any of these bits are at "1", the device will not function properly.

**More Information**

DS3134: QuickView -- Full (PDF) Data Sheet -- Free Samples